What is claimed is:

1. A wafer, comprising:

at least two die areas formed on the wafer, the at least two die areas defining a street therebetween; and

a stress migration test structure in the street, the stress migration test structure capable of detecting stress migration voids.

2. A wafer, comprising:

at least four die areas formed on the wafer, the at least four die areas defining two intersecting streets thereamong; and

a stress migration test structure capable of detecting stress migration voids, the stress migration test structure in a region of the two intersecting streets proximate the at least four die areas.

3. A stress migration test device, comprising:

a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at uniform impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress migration void in the runner is a detectable portion of the impedance between the adjacent taps absent stress migration voids.

4. A stress migration test device as recited in claim 3, wherein the conductive runner defines a width that is the minimum line width for the technology in which the runner is fabricated.

5. A stress migration test device as recited in claim 3, wherein the conductive runner defines a length that is at least 100 micrometers long.

6. A stress migration test device as recited in claim 3, wherein the conductive runner defines a length that is at least 400 micrometers long.

7. A stress migration test device as recited in claim 3, wherein the distance between adjacent ones of the plurality of taps encompasses at least ten crystallographic grains of the material of which the conductive runner is fabricated.

8. A stress migration test device as recited in claim 3, wherein tap conductors extending from the conductive runner to taps are of the same linewidth as the conductive runner.

9. A stress migration test device as recited in claim 3, wherein the conductive runner is comprised of two conductive materials providing parallel conduction paths of different impedances.

10. A stress migration test device as recited in claim 3, wherein the conductive runner extends unidirectionally.

11. A stress migration test device as recited in claim 3, wherein the conductive runner serpentines back and forth boustrophedonically.

12. A stress migration test device as recited in claim 3, wherein the conductive runner is fabricated on at least two levels of interconnects.

13. A chip, comprising:

a substrate having circuits within an area for circuit layout;

bond pads on the substrate along at least one edge of the chip, the bond pads being between the area for circuit layout and the at least one edge of the chip; and

a stress migration test device fabricated as part of the chip, the stress migration test device comprising a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at uniform impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress migration void in the conductive runner is a detectable portion of the impedance between the adjacent taps absent stress migration voids.

14. A chip as recited in claim 13, wherein the stress migration test device is fabricated in a layer beneath the layer in which the bond pads are fabricated.

15. A chip as recited in claim 14, packaged as an integrated circuit.

16. A chip as recited in claim 13, wherein the stress migration test device is fabricated between the bond pads and the at least one edge of the chip.

17. A chip as recited in claim 16, packaged as an integrated circuit.

18. A chip as recited in claim 13, wherein the stress migration test device is fabricated between the bond pads and the area for circuit layout.

19. A chip as recited in claim 18, packaged as an integrated circuit.

20. A chip as recited in claim 13, wherein the stress migration test device is fabricated within the area for circuit layout.

21. A chip as recited in claim 20, packaged as an integrated circuit.

22. A chip, comprising:

a substrate having circuits within an area for circuit layout;

bond pads on the substrate along at least one edge of the chip, the bond pads being between the area for circuit layout and the edge of the chip; and

at least a portion of a stress migration test device fabricated between the bond pads and the at least one edge of the chip, the stress migration test device comprising a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at uniform impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress migration void in the conductive runner is a detectable portion of the impedance between the adjacent taps absent stress migration voids.

23. A chip as recited in claim 22, wherein the conductive runner extends unidirectionally.

24. A chip as recited in claim 22, wherein the conductive runner serpentines back and forth boustrophedonically.

25. A chip as recited in claim 22, wherein at least a portion of a stress migration test device is fabricated between the bond pads and more than one edge of the chip.

26. A chip as recited in claim 22, packaged as an integrated circuit.

27. A chip as recited in claim 22, wherein the conductive runner of the at least a portion of a stress migration test device is fabricated in more than one level of metal.

28. A chip as recited in claim 22, wherein the conductive runner of the at least a portion of a stress migration test device is comprised of two conductive materials providing parallel conduction paths of different impedances.

29. A stress migration test device, comprising:

a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress migration void in the runner is a detectable portion of the expected impedance between the adjacent taps absent stress migration voids.

30. A stress migration test device as recited in claim 29, wherein the conductive runner is comprised of two conductive materials providing parallel conduction paths of different impedances.

31. A stress migration test device as recited in claim 29, wherein the conductive runner is fabricated on at least two levels of interconnects.

32. A chip, comprising:

a substrate having circuits within an area for circuit layout;

bond pads on the substrate along at least one edge of the chip, the bond pads being between the area for circuit layout and the at least one edge of the chip; and

a stress migration test device fabricated as part of the chip, the stress migration test device comprising a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress

migration void in the conductive runner is a detectable portion of the expected impedance between the adjacent taps absent stress migration voids.

33. A chip, comprising:

a substrate having circuits within an area for circuit layout;

bond pads on the substrate along at least one edge of the chip, the bond pads being between the area for circuit layout and the edge of the chip; and

at least a portion of a stress migration test device fabricated between the bond pads and the at least one edge of the chip, the stress migration test device comprising a conductive runner, the conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated, the conductive runner having a plurality of taps at impedance intervals along the runner, the taps spaced along the runner such that the variation of impedance of the runner between adjacent taps due to presence of a stress migration void in the conductive runner is a detectable portion of the expected impedance between the adjacent taps absent stress migration voids.

34. A method of determining the presence or absence of stress migration voids in a conductor, comprising the steps of:

fabricating on a substrate a conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated;

providing taps at equal impedance intervals along the runner;

passing a known current through a first portion of the conductive runner between two spaced taps;

measuring the voltage developed across a second portion of the conductive runner due to the known current, the second portion of the conductive runner being a subset of the first portion of the conductive runner;

calculating an impedance of the second portion of the conductive runner;

normalizing the impedance of the second portion of the conductive runner by a nominal impedance to generate an impedance ratio; and

comparing the impedance ratio to an impedance ratio threshold to determine whether a stress migration void is present in the second portion of the conductive runner.

35. A method as recited in claim 34, further comprising the steps of:

indexing the two spaced taps defining the first portion of the conductive runner to define a new first portion of the conductive runner;

passing a known current through the new first portion of the conductive runner; and

developing an impedance of a new second portion of the conductive runner, the new second portion of the conductive runner being a subset of the new first portion of the conductive runner.

36. A method as recited in claim 35, further comprising the step of:

repeating the indexing, current passing and impedance developing steps until an impedance has been developed for all second portions of the conductive runner.

37. A method as recited in claim 36, further comprising the step of:

generating the nominal impedance from the impedances developed for the second portions of the conductive runner.

38. A method as recited in claim 37, wherein generating a nominal impedance from the impedances developed for the second portions of the conductive runner comprises generating the nominal impedance as an average of the impedances developed for the second portions of the conductive runner.

39. A method of determining the presence or absence of stress migration voids in a conductor, comprising the steps of:

fabricating on a substrate a conductive runner having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated;

providing taps at impedance intervals along the runner;

passing a known current through a first portion of the conductive runner between two spaced taps;

measuring the voltage developed across a second portion of the conductive runner due to the known current, the second portion of the conductive runner being a subset of the first portion of the conductive runner;

calculating an impedance of the second portion of the conductive runner;

normalizing the impedance of the second portion of the conductive runner by an expected impedance for the second portion of the conductive runner to generate an impedance ratio; and

comparing the impedance ratio to an impedance ratio threshold to determine whether a stress migration void is present in the second portion of the conductive runner.

40. A method as recited in claim 39, further comprising the steps of:

indexing the two spaced taps defining the first portion of the conductive runner to define a new first portion of the conductive runner;

passing a known current through the new first portion of the conductive runner; and

developing an impedance of a new second portion of the conductive runner, the new second portion of the conductive runner being a subset of the new first portion of the conductive runner.

41. A method as recited in claim 40, further comprising the step of:

repeating the indexing, current passing and impedance developing steps until an impedance has been developed for all second portions of the conductive runner.